REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 8, 16, 17, 24 and 27-38 have been amended. Thus, claims 1-38 are currently pending in the application and subject to examination.

Informal Matters

In the Office Action mailed October 24, 2007, claims 1-15 were rejected under 35 U.S.C. § 112, first paragraph and claims 8-10, 24-26 and 35-37 were rejected under 35 U.S.C. § 112, second paragraph. Claims 9-10, 25-26 and 36-37 were rejected based on their dependency on their respective intermediate and parent claims which are rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 8, 17, 24 and 35 have been amended responsive to these rejections. If any additional amendment is necessary to overcome the rejections, the Examiner is requested to contact the Applicant's undersigned representative.

REJECTION UNDER 35 U.S.C. § 101

Claims 1-16, 28-37 and 38 were rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. Claims 1, 16 and 28-38 have been amended responsive to these rejections. If any additional amendment is necessary to overcome the rejections, the Examiner is requested to contact the Applicant's undersigned representative.

REJECTION UNDER 35 U.S.C. § 103(a)

Claims 1-7, 13-14, 16-23, 27-34 and 38 were rejected under 35 U.S.C. § 103(a)

as being unpatentable over Yook (Jong-Kwan Yook et al., "Computation of Switching Noise in Printed Circuit Boards", 1997, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Volume 20, Number 1, March 1997, pages 64-75) in view of Harada, U.S. Patent No. 6,557,154 (hereinafter, "6,557,154). Claims 8-10, 24-26, 35-37 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yook as modified by Harada as applied to claims 1-7, 13-14, 16-23, 27-34 and 38 above, and further in view of Shi (Hao Shi et al., "Modeling Multilayed PCB Power-Bus Designs Using an MPIE Based Circuit Extraction Technique", August 1998, IEEE International Symposium on Electromagnetic Compatibility, pages 647-651). Claims 11-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yook as modified by Harada as applied to claims 1-7, 13-14, 16-23, 27-34 and 38 above, and further in view of Papadopoulou, U.S. Patent No. 6,178,539 (hereinafter, "Papadopoulou"). It is noted that claims 1, 8, 16, 17, 24 and 27-38 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

In the Applicants invention as recited in independent claim 1, as amended, a power supply pair extraction processing section extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the entire circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands across the entire circuit board are extracted by the

power supply pair extraction processing section. Thus, in the claimed invention, all areas across the circuit board are considered when the power supply pairs are extracted.

In making the rejections of independent claims 1, 17 and 28, the Examiner asserts that Yook teaches all of the features in claims 1, 17 and 28 with the exception of a CAD data obtaining section that obtains CAD data including information concerning a board shape, pattern shapes, and elements; and a CAD data conversion processing section that converts said CAD data into power supply island pattern data, element data, lead pattern data, and via pattern data; from the CAD data. The Examiner asserts that Yook teaches the remaining features of claims 1, 17 and 28 in various sections of pages 66-69 and in Figs. 2 and Fig. 3. See, Office Action, page 11.

In making the rejections of independent claims 16, 27 and 38, the Examiner asserts that Yook teaches all of the features in claims 16, 27 and 38 with the exception of a power supply pair extraction processing section that extracts, as a power supply pair, different two power supply layers overlapping each other in a layering direction from data indicative of said circuit board. The Examiner asserts that Yook teaches the remaining features of claims 16, 27 and 38 at page 64, Fig. 2; page 68; Fig. 3; page 64, right- side column, second paragraph that starts with, "The goal of..."; page 67, left-side column, last paragraph, and right-side column, second paragraph that starts with, "For PCB's having..."; and page 68, right-side column. See, Office Action, pp. 13 and 14.

However, the Applicant notes that the cited sections of Yook disclose a method of modeling and analyzing simultaneous switching noise in printed circuit boards using a traditional mesh/SPICE approach and do not disclose or suggest at least the features of

a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands, across the circuit board, are extracted by the power supply pair extraction processing section, as recited in claim 1, as amended.

None of Harada, Shi and Papadopoulou, alone or in any combination thereof, discloses or suggests at least the features of a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the entire circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands across the entire circuit board are extracted by the power supply pair extraction processing section, as recited in claim 1, as amended.

For at least these reasons, the Applicants submit that claim 1 is allowable over the applied art of record. As claim 1 is allowable, the Applicants submit that claims 2-15, which depend from allowable claim 1, are likewise allowable for at least the reasons set forth above with respect to claim 1.

For similar reasons as those set forth above with respect to claim 1, the Applicants submit that each of independent claims 16, 17, 27, 28 and 38, as amended, are allowable over the applied art of record. As amended claims 17 and 28 are allowable, the Applicant submits that claims 18-26 and 29-37, which depend from allowable claims 17and 28, respectively, are likewise allowable for at least the reasons set forth above with respect to claim 1, 17 and 28.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1-38 are in condition for allowance and a Notice of Allowability is earnestly solicited.

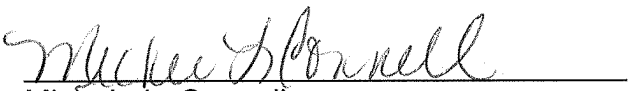
Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this

communication to Deposit Account No. 01-2300 referencing client matter number 024938-00002.

Respectfully submitted,

Arent Fox LLP



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Enclosures: Request for Continued Examination